REMARKS

Claims 1-5 were examined and reported in the Office Action. Claims 1-5 are rejected. Claim 5 is cancelled. Claims 1-4 are amended. New claim 6 is added. Claims 1-4 and 6 remain. Applicant requests reconsideration of the application in view of the following remarks.

I. Specification Objections

It is asserted in the Office Action that the Abstract and disclosure are objected to for clarity. Applicant has amended the abstract and the disclosure to overcome the asserted objections.

Accordingly, withdrawal of the specification objections are respectfully requested.

II. Claim Objections

It is asserted in the Office Action that claims 1-3 are objected to for various informalities. Applicant has amended claims 1-3 to overcome the informal objections.

Accordingly, withdrawal of the informal claim objections are respectfully requested.

III. 35 U.S.C. §112

A. It is asserted in the Office Action that claim 3 is rejected under 35 U.S.C. §112, first paragraph as failing to comply with the enablement requirement. Applicant has amended claim 3 to overcome the 35 U.S.C. §112, first paragraph rejection.

Accordingly, withdrawal of the 35 U.S.C. §112 rejection for claim 3 is respectfully requested.

B. It is asserted in the Office Action that claims 1-5 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the submet matter which applicant regards as the invention. Applicant has amended claims 1-4 and canceled claim 5 to overcome the 35 U.S.C. §112, second paragraph rejections.

Accordingly, withdrawal of the 35 U.S.C. §112, second paragraph rejections for claims 1-5 are respectfully requested.

IV. 35 U.S.C. §102(e)

A. It is asserted in the Office Action that claims 1-3 are rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent 6,557,080 issued to Burger ("Burger"). Applicant respectfully traverses the aforementioned rejection for the following reasons.

According to MPEP §2131,

> '[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.' (Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987)). 'The identical invention must be shown in as complete detail as is contained in the ... claim.' (Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)). The elements must be arranged as required by the claim, but this is not an ipsissimis verbis test, *i.e.*, identity of terminology is not required. (In re Bond, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990)).

Applicant's amended claim 1 contains the limitations of

> [a] semiconductor memory device, comprising: a cell area having N+1 number of unit cell blocks, each including M number of word lines wherein the N number of unit cell blocks are each corresponded to a logical cell block address and one unit cell block is added for accessing data with high speed; a predetermined cell block table for storing candidate information representing at least more than one candidate word line among the M * (N+1) number of the word lines; and a tag block for receiving a row address, sensing the logical cell block address in the row address and outputting a physical cell block address based on the logical cell block address and the candidate information, wherein the tag block includes:N+1 number of unit tag tables corresponding to the N+1 number of unit cell blocks, each having M number of registers, the M number of registers corresponding to M number of word lines of

corresponding unit cell blocks, each register storing one logical cell block address; and an initialization unit for initializing the N+1 number of unit tag tables.

Burger discloses a cache structure for computer architecture that evaluates the subblocks actually used in the cache to modify the granularity of subsequent refreshes of the cache. It is noted that the Office Action does not assert specific reasons or where in Burger are Applicant's claim limitations disclosed. It is implied in the Office Action that Applicant's claimed tag block corresponds to a tag memory 28 disclosed in Burger. Burger, however, does not teach, disclose or suggest a cell area having N+1 number of unit cell blocks, each including M number of word lines wherein the N number of unit cell blocks are each corresponded to a logical cell block address and one unit cell block is added for accessing data with high speed. The tag block of Applicant's claimed invention is arranged for controlling the N+1 number of unit cell blocks. Further, in order to initialize the N+1 number of unit tag tables, Applicant's claimed invention has an initialization unit of the tag block. The memory circuit of Burger only has memory cell blocks corresponded to an address and does not have an additional memory cell block added for accessing data with high speed.

Therefore, since Burger does not disclose, teach or suggest all of Applicant's amended claim 1 limitations, Applicant respectfully asserts that a *prima facie* rejection under 35 U.S.C. § 102(e) has not been adequately set forth relative to burger. Thus, Applicant's amended claim 1 is not anticipated by Burger. Additionally, the claims that directly or indirectly depend on claim 1, namely claims 2-3, are also not anticipated by Burger for the same reason.

Accordingly, withdrawal of the 35 U.S.C. §102(e) rejection for claims 1-3 is respectfully requested.

B. It is asserted in the Office Action that claim 4 is rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Publication 2004/0153793 A1 by Jarboe ("Jarboe"). Applicant respectfully traverses the aforementioned rejection for the following reasons.

Applicant's amended claim 4 contains the limitations of

> [a] method for controlling a tag block for assigning a physical unit cell address based on a logical unit cell block, comprising: initializing the tag block in a semiconductor memory device; and performing a data access operation of the semiconductor memory device by using the tag block, wherein the initializing the tag block in a semiconductor memory device including: nullifying a N+1 number of unit tag tables of the tag block; selecting all the N+1 number of unit tag tables; and storing each different logical unit cell block information in the N number of unit tag tables among the N+1 number of unit tag tables.

Jarboe discloses a method and apparatus for testing memory arrays. Jarboe discloses initializing a tag row when repairing failing memory locations. Jarboe, however, does not teach, disclose or suggest

> controlling a tag block for assigning a physical unit cell address based on a logical unit cell block, comprising: initializing the tag block in a semiconductor memory device; and performing a data access operation of the semiconductor memory device by using the tag block, wherein the initializing the tag block in a semiconductor memory device including: nullifying a N+1 number of unit tag tables of the tag block; selecting all the N+1 number of unit tag tables; and storing each different logical unit cell block information in the N number of unit tag tables among the N+1 number of unit tag tables.

Therefore, since Jarboe does not disclose, teach or suggest all of Applicant's amended claim 4 limitations, Applicant respectfully asserts that a *prima facie* rejection under 35 U.S.C. § 102(e) has not been adequately set forth relative to Jarboe. Thus, Applicant's amended claim 4 is not anticipated by Jarboe.

Accordingly, withdrawal of the 35 U.S.C. §102(e) rejection for claim 4 is respectfully requested.

V. 35 U.S.C. §103(a)

It is asserted in the Office Action that claim 5 is rejected under 35 U.S.C. §103(a) as being unpatentable over Jarboe and in further view of U. S. Patent No. 5,584,003 issued to

Yamaguchi et al. ("Yamaguchi"). Applicant has canceled claim 5. Therefore the aforementioned 35 U.S.C. §103(a) rejection is moot.

VI. Double Patenting

The Office Action rejects the application for nonstatutory double patenting and states that a timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d)may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned. Applicant respectfully traverses the aforementioned rejection for the following reasons.

Applicant's amended claim 1 is absolutely different from claim 42 of US10/696,144. That is, amended claim 1 is focused on initializing the tag block. Claim 42 of US10/696,144 does not assert initializing of the tag block. Further, claim 42 does not include limitations of the tag block includes an initialization unit for initializing the N+1 number of unit tag tables.

Accordingly, withdrawal of the nonstatutory rejection for claims 1-3 is respectfully requested.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending, namely 1-4 and 6, patentably define the subject invention over the prior art of record and are in condition for allowance and such action is earnestly solicited at the earliest possible date.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly extension of time fees. If a telephone interview would expedite the prosecution of this Application, the Examiner is invited to contact the undersigned at (310) 207-3800.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

Dated: May 11, 2006

By: _____
Steven Laut, Reg. No. 47,736

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025
(310) 207-3800

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail with sufficient postage in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P. O. Box 1450, Alexandria, Virginia 22313-1450 on May 11, 2006.

_____
Jean Svoboda